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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,746	07/24/2003	Hatsuki Kanbayashi	115816	8139

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EXAMINER
MAGEE, THOMAS J

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EIC

Office Action Summary	Application No.	Applicant(s)	
	10/625,746	KANBAYASHI, HATSUKI	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections – 35 U.S.C. 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 – 4, 6, 9, 10, 13, and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Bertin et al. (US 5,502,667).

3. Regarding Claim 1, Bertin et al. disclose a method of manufacturing a semiconductor device, comprising:

mounting a semiconductor chip (14) (Figure 2) having electrodes on a substrate (18) having wiring patterns (connection terminals) (25A,25B), and

forming conductive layers (20) (on 21) that electrically connect the electrodes and the wiring patterns (Col. 4, line 66 through Col. 5, line1) in a manner such that the conductive layers are disposed on side surfaces of the semiconductor chip..

4. Regarding Claims 2, 4,and 10, Bertin et al. disclose (See Figure 2) that the chips are bonded "face-up." (Col. 5, lines 39 – 41).

5. Regarding Claim 3, Bertin et al. disclose a method of manufacturing a semiconductor device, comprising:

stacking in layers a plurality of semiconductor chips (14) having electrodes on a substrate (18) having wiring patterns (connection terminals) (25A,25B), and

forming conductive layers (20) (on 21) that electrically connect the electrodes and the wiring patterns (Col. 4, line 66 through Col. 5, line1) in a manner such that the conductive layers are disposed on a side surfaces of at least one of the semiconductor chips.

6. Regarding Claims 5 and 11, Bertin et al. disclose a method of manufacturing a semiconductor device, further including mounting a second semiconductor chip (22) that is smaller than a first semiconductor chip among the plurality of semiconductor chips (14) on the first semiconductor chip.

7. Regarding Claim 6, Bertin et al. disclose forming a second conductive layer (Col. 4, line 66 through Col. 5, line1) that electrically connects the electrodes of one of the semiconductor chips and the electrodes of another of the semiconductor chips in a manner to pass a side surface of at least one of the semiconductor chips.

8. Regarding Claims 7 and 12, Bertin et al. do not explicitly disclose that a first semiconductor chip is face down bonded among a plurality of face-up bonded chips, wherein face-up bonding of a second semiconductor chip to a side of the first semiconductor chip opposite to a side

where the electrodes are formed. However, Bertin et al. do disclose that the smaller "logic chip" can be mounted at the bottom (Col. 12, lines 53 – 59) such that the chip is mounted face-down and bonded to the overlying (second) semiconductor chip bonded face-up, wherein the side is opposite to that where the electrodes are formed. It is therefore implicit that the first chip is bonded face down among a plurality of face-up bonded chips and that the first chip is bonded to a second chip that is bonded face-up, opposite to a side where electrodes are formed.

9. Regarding Claim 9, Masayuki et al. disclose a semiconductor device, comprising:

a substrate (18) having wiring patterns (25A, 25B),

a plurality of stacked semiconductor chips (14) having electrodes,

a conductive layer (20) that electrically connects the electrodes of any one of the semiconductor chips and the wiring patterns in a manner to pass a side surface of at least one of the semiconductor chips, and

a second conductive layer (Col. 4, line 66 through Col. 5, line1) that electrically connects the electrodes of one of the semiconductor chips and the electrodes (at 6) of another of the semiconductor chips in a manner to pass a side surface of at least one of the semiconductor chips.

10. Regarding Claim 13, Bertin et al. disclose (Col. 2, lines 23 – 58) a circuit assembly on a substrate with the semiconductor device mounted therein.

11. Regarding Claim 14, Bertin et al. do not explicitly disclose a piece of electronic equipment where the device would be used, but it is inherent that the device would be utilized in a piece of electronic equipment, including any application where memory devices are required, for example, a personal computer.

Claim Rejections – 35 U.S.C. 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obvious-ness rejections set forth in this Office Action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bertin et al., as applied to Claims 1 – 7, and 9 – 14, and further in view of Moon (US 6,566,739 B2).

14. Regarding Claim 8, Bertin et al. do not disclose a method for forming a conductive layer by ejecting a solution containing fine particles. Moon discloses a technique for forming conductive traces (Figure 6), wherein a solution (81c) is ejected from a dispenser (93) (Col. 6, lines 16 – 26). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the procedures of Moon in Bertin et al. to provide an efficient means of forming conductive layer traces.

Response to Arguments

15. Arguments of Applicant with respect to claim rejections have been carefully considered, but these have been found to be unpersuasive. In particular, arguments are based on limitations of the amended claims and have been discussed in detail in the Office Action. Further, arguments are considered moot in terms of the new ground(s) of rejection.

Conclusion

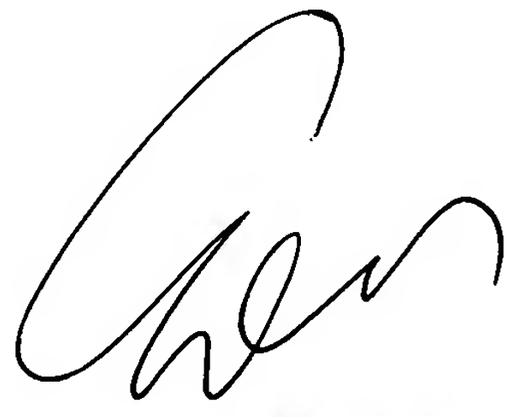
16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The

Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST).

If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**



EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Thomas Magee
March 14, 2005